Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the Specification.

Listing of Claims:

1-8. (Canceled)

9. (Currently amended) ~~The serializer of claim 4,~~ A serializer for converting *N*-bit wide parallel input data words with rate *B* into a serial data bit stream with rate *NB* of out-going serial words, comprising:

a first multiplexer with ratio *N*:*L* for conversion of the *N*-bit wide parallel input data words with rate *B* into *L*-bit wide data words with rate *NB/L*;

a converter for generating encoded data words from the *L*-bit wide data words;

a second multiplexer with ratio *L*:1 for conversion of the encoded data words with rate *NB/L* into a serial data bit stream with rate *NB*;

a multilevel buffer for generating a multilevel output signal with marking pulses using the serial bit data stream and a synchronization signal; and

a timing circuit for generating the synchronization signal,

wherein the multilevel buffer further comprises:

a retiming sub-block for conversion of *L*-bit long synchronization pulses into 1-bit long retimed synchronization pulses; and

a single-ended current-switching stage for generating a multilevel serial data signal in which an amplitude of a bit coincident with a synchronization pulse and having a preselected logic value is increased.

10. (Original) The serializer of claim 9, wherein the single-ended current-switching stage is for a preselected logic value of "1", the serializer further comprising:

a first current source for generation of a first current;

a second current source for generation of a second current with the same value as the first current;

a first single-pole/single-throw switch coupled to the first current source and being closed by a direct input data signal;

a second single-pole/single-throw switch coupled to the second current source and being closed by an inverted input data signal;

a third single-pole/single-throw switch coupled to the output of the first single-pole/single-throw switch and being closed by an inverted synchronization signal;

a first resistor coupling the output of the third single-pole/single-throw switch with a positive power supply node; and

a second resistor coupling the output of the third single-pole/single-throw switch with the output of the second single-pole/single-throw switch serving as the stage output.

11. (Currently amended) ~~The serializer of claim 4,~~ A serializer for converting *N*-bit wide parallel input data words with rate *B* into a serial data bit stream with rate *NB* of out-going serial words, comprising:

a first multiplexer with ratio *N*:*L* for conversion of the *N*-bit wide parallel input data words with rate *B* into *L*-bit wide data words with rate *NB/L*;

a converter for generating encoded data words from the *L*-bit wide data words;

a second multiplexer with ratio *L*:1 for conversion of the encoded data words with rate *NB/L* into a serial data bit stream with rate *NB*;

a multilevel buffer for generating a multilevel output signal with marking pulses using the serial bit data stream and a synchronization signal; and

a timing circuit for generating the synchronization signal,

wherein the multilevel buffer further comprises:

a retiming sub-block for generating 1-bit long retimed synchronization pulses using *L*-bit long synchronization pulses and for retiming and delay of the incoming serial data bit stream; and

a differential current-switching stage for generating direct and inverted two logic level serial data signals wherein the amplitude of a bit coincident with the synchronization pulse and having a preselected logic value is increased to a third logic level.

12. (Original) The serializer of claim 11, wherein the differential current-switching stage for a preselected logic value of "1" further comprises:

a first current source for generation of a first current;

a second current source for generation of a second current with the same value as the first current;

a first single-pole/double-throw switch with its input coupled to the first current source and shorted to its first output by a direct input data signal;

a second single-pole/double-throw switch with its input coupled to the second current source and shorted to its first output by an inverted input data signal;

a first single-pole/single-throw switch coupled to the first output of the first single-pole/double-throw switch and being closed by an inverted synchronization signal;

a second single-pole/single-throw switch coupled to the second output of the first single-pole/double-throw switch and being closed by an inverted synchronization signal;

a first resistor coupling an output of the first single-pole/single-throw switch to a positive power supply node;

a second resistor coupling the output of the first single-pole/single-throw switch with the first output of the second single-pole/double-throw switch serving as the stage direct output;

a third resistor coupling the output of the second single-pole/single-throw switch with the same positive power supply node; and

a fourth resistor connecting the output of the second single-pole/single-throw switch with the second output of the second single-pole/double-throw switch serving as the stage inverted output.

13. (Canceled)

14. (Currently amended) ~~The deserializer circuit of claim 13,~~ A deserializer circuit for generating *N*-bit wide parallel data words with rate *B* and a predetermined bit order from an incoming serial data bit stream with rate *NB*, comprising:

a timing circuit for generating timing signals using marking pulses imposed onto the incoming serial data stream, and for generating a serial data stream with rate *NB*;

a first demultiplexer with ratio 1:*L* for generating *L*-bit wide data words with rate *NB/L* using the serial data stream;

a data digital converter for generating decoded data words using the *L*-bit wide data words; and

a second demultiplexer with ratio *L*:*N* for converting the decoded data words into *N*-bit wide parallel data words with rate *B* and a bit order predetermined by the alignment of the timing signals to the marking pulses,

wherein the timing circuit further comprises:

a single-ended input detector for accepting the incoming serial data bit stream and retrieving data bits and synchronization pulses corresponding to the marking pulses, comprising:

a single-ended input buffer for impedance matching;

a single-ended pick sensor for detecting a maximum voltage level and a minimum voltage level of the input signal;

a voltage divider for generating a first threshold voltage and a second threshold voltage using the detected voltage levels;

a first comparator for retrieving synchronization pulse values in reference to the first threshold voltage; and

a second comparator for retrieving data bit values in reference to the second threshold voltage.

15. (Currently amended) ~~The deserializer circuit of claim 13,~~ A deserializer circuit for generating *N*-bit wide parallel data words with rate *B* and a predetermined bit order from an incoming serial data bit stream with rate *NB*, comprising:

a timing circuit for generating timing signals using marking pulses imposed onto the incoming serial data stream, and for generating a serial data stream with rate *NB*;

a first demultiplexer with ratio 1:*L* for generating *L*-bit wide data words with rate *NB/L* using the serial data stream;

a data digital converter for generating decoded data words using the *L*-bit wide data words; and

a second demultiplexer with ratio *L*:*N* for converting the decoded data words into *N*-bit wide parallel data words with rate *B* and a bit order predetermined by the alignment of the timing signals to the marking pulses,

wherein the timing circuit further comprises:

a single-ended input detector for accepting the incoming serial data bit stream and retrieving data bits and synchronization pulses corresponding to the marking pulses, comprising:

a single-ended input buffer for impedance matching;

a first comparator for retrieving synchronization pulse values in reference to a first external threshold voltage; and

a second comparator for retrieving data bit values in reference to a second external threshold voltage.

16. (Currently amended) ~~The deserializer circuit of claim 13,~~ A deserializer circuit for generating *N*-bit wide parallel data words with rate *B* and a predetermined bit order from an incoming serial data bit stream with rate *NB*, comprising:

a timing circuit for generating timing signals using marking pulses imposed onto the incoming serial data stream, and for generating a serial data stream with rate *NB*;

a first demultiplexer with ratio 1:*L* for generating *L*-bit wide data words with rate *NB/L* using the serial data stream;

a data digital converter for generating decoded data words using the *L*-bit wide data words; and

a second demultiplexer with ratio *L:N* for converting the decoded data words into *N*-bit wide parallel data words with rate *B* and a bit order predetermined by the alignment of the timing signals to the marking pulses,

wherein the timing circuit further comprises:

a differential input detector for accepting incoming direct and inverted serial data bit streams with imposed marking pulses and retrieving data bits and synchronization pulses corresponding to the marking pulses, comprising:

a differential input buffer for impedance matching;

a differential pick sensor for detecting a maximum voltage level and a minimum voltage level of the input signal;

a voltage divider for generating a first threshold voltage using the detected voltage levels;

a differential comparator for retrieving synchronization pulse values from both direct and inverted input bit streams in reference to the first threshold voltage; and

a limiting amplifier with two standard output voltage levels for reconstruction of data bit values.

17. (Currently amended) ~~The deserializer circuit of claim 13,~~ A deserializer circuit for generating *N*-bit wide parallel data words with rate *B* and a predetermined bit order from an incoming serial data bit stream with rate *NB*, comprising:

a timing circuit for generating timing signals using marking pulses imposed onto the incoming serial data stream, and for generating a serial data stream with rate *NB*;

a first demultiplexer with ratio 1:*L* for generating *L*-bit wide data words with rate *NB/L* using the serial data stream;

a data digital converter for generating decoded data words using the *L*-bit wide data words; and

a second demultiplexer with ratio *L*:*N* for converting the decoded data words into *N*-bit wide parallel data words with rate *B* and a bit order predetermined by the alignment of the timing signals to the marking pulses,

wherein the timing circuit further comprises:

a differential input detector for accepting incoming direct and inverted serial data bit streams with imposed marking pulses and retrieving data bits and synchronization pulses corresponding to the marking pulses, comprising:

a differential input buffer for impedance matching;

a differential comparator for retrieving synchronization pulse values from both direct and inverted input bit streams in reference to an external threshold voltage; and

a limiting amplifier with two standard output voltage levels for reconstruction of data bit values.